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APR 25

Sheet 1 of 1

Application Number	10/666,765
Filing Date	Sep. 17, 2003
First Named Inventor	Mahesh A. Iyer
Art Unit	2184 2119
Examiner Name	Jesup P. Hiru
Attorney Docket Number	06816.0506CON1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
H	1	A. Aharon, A. Bar-David, B. Dorfman, E. Gofman, M. Leibowitz, and V. Schwartzburd, "Verification of the IBM RISC System/6000 by a Dynamic Biased Pseudo-Random Test Program Generator", IBM Systems Journal, Vol. 30, No. 4, 1991, pp. 527-538.	
H	2	E. Bin, R. Emek, G. Shurek, and A. Ziv, "Using a Constraint Satisfaction Formulation and Solution Techniques for Random Test Program Generation", IBM Systems Journal, Vol. 41, No. 3, 2002, pp. 386-400.	
H	3	A. K. Chandra and V. S. Iyengar, "Constraint Solving for Test Case Generation", Proceedings of International Conference on Computer Design, 1992, pp. 245-248.	
H	4	A. K. Chandra, V. S. Iyengar, D. Jameson, R. Jawalekar, I. Nair, B. Rosen, M. Mullen, J. Yoon, R. Armoni, D. Geist, and Y. Wolfsthal, "AVPGEN - A Test Case Generator for Architecture Verification", IEEE Transactions on VLSI Systems, Vol. 3, No. 2, June 1995, pp. 188-200.	
H	5	C.-Y. Huang and K.-T. Cheng, "Assertion Checking by Combined Word-level ATPG and Modular Arithmetic Constraint-Solving Techniques", Proceedings of the Design Automation Conference, June 2000.	
H	6	M. A. Iyer, "High Time for High-Level ATPG", Panel position statement, Proceedings of the International Test Conference, 1999, pp. 1112.	
H	7	W. Kunz, and D. Pradhan, "Recursive Learning: A New Implication Technique for Efficient Solutions to CAD-problems - Test, Verification and Optimization", IEEE Transactions on Computer-Aided Design, Vol. 13, No. 9, September 1994, pp. 1143-1158.	
H	8	I. Yuan, K. Shultz, C. Pixley, H. Miller, and A. Aziz, "Modeling Design Constraints and Biasing in Simulation Using BDDs", Proceedings of the International Conference on Computer-Aided Design, November 1999, pp. 584-589.	

Examiner Signature		Date Considered	12/7/05
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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